

Charge injection across a metal-organic interface suppressed by thermal diffusion

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We find that the ohmic conductance of Co-phthalocyanine (CoPc) vertical capacitive devices is irreversibly suppressed by orders of magnitude when they are heated above 340 K. Detailed structural and transport studies imply that the changes in the conductance are due to diffusion of the top Pd electrode into the CoPc layer. This leads to a decrease in Pd electrode effective work function, which increases the potential barrier for hole injection. © 2014 AIP Publishing LLC. [http://dx.doi.org/10.1063/1.4863205]

Metallo-phthalocyanines (MPcs) are molecular semiconductors with interesting structural,^{1–4} optical,^{5–8} and electrical properties.⁹ MPc-based devices have been studied for applications in solar cells,^{10–12} organic light-emitting diodes (OLEDs),^{13–15} chemical sensors,^{16–20} and organic field effect transistors (OFETs).^{16–18,20,21} Considerable progress has been made in developing MPc devices, although details of the underlying mechanisms in electrical transport are not fully understood. More importantly, few studies have explored their performance under realistic operational conditions,²² i.e. working temperatures above room temperature.

Below room temperature, the conductance in the ohmic regime of CoPc and CuPc capacitive devices decreases exponentially with organic layer (OL) thickness and increases exponentially with temperature.²³ This can be understood with the thermally assisted sequential tunneling (TAST) model, which separates contributions to electrical transport from the electrode-OL interfaces and the bulk OL. Recently, this model was expanded to include the effect of OL roughness and micro-shorts between electrodes.²⁴ However, mechanisms that affect the electrode-OL interface, especially above 300 K, are poorly understood.

In this Letter, we explore the performance of organic capacitive devices under technologically relevant operation conditions (i.e. T > 300 K). Conductivities of CoPc capacitive devices with Pd electrodes (Fig. 1, inset) deviate from the expected exponential temperature dependence when heated above 340 K. Upon cooling, the devices remain irreversibly in a 3 orders of magnitude more resistive state, but the exponential behavior is recovered. Specular x-ray reflectometry (XRR) shows that this change correlates with a temperature dependent diffusion of the top electrode into the OL. This diffusion is also consistent with the appearance of additional microshorts²⁴ in thin OLs. The increased roughness due to interdiffusion, combined with the crystallographic dependence of the electrode work function, 2^{2-28} leads to an effective increase in the potential barrier for hole injection into the OL from the top electrode. This conclusion

^{a)}Author to whom correspondence should be addressed. Electronic mail: cmonton@physics.ucsd.edu. is based on an exhaustive study of more than ten transport devices and x-ray diffraction (XRD) in seven multilayers.

Capacitive devices with organic layer thicknesses of 35 nm to 135 nm were grown in an organic molecular beam epitaxy (OMBE) system with a 1×10^{-10} Torr base pressure using CoPc powder which was triple purified by gradient sublimation. 40 nm-100 nm thickness Pd bottom (BE) and top electrodes (TE), respectively, were deposited by electron beam deposition. The OL was deposited using a Knudsen effusion cell with a specially designed heated lip. The deposition rates for the BE and the OL were 0.3 Å/s and 0.4 Å/s, respectively. The TE was deposited at a higher rate (10 Å/s)to favor formation of larger, less mobile metal clusters which decreases the diffusion into the OL at room temperature.²⁹ The devices were exposed to air for 1 h to place contacts for transport measurements. Oxygen induced effects³⁰ were minimized by including a 4 day stabilization period in high-vacuum at room temperature prior to each measurement. During this period, the current was monitored, and the measurement started only after a complete flattening of the curve was observed. DC current-voltage measurements were performed in a two-probe configuration in darkness and



FIG. 1. Normalized conductivity (G/A) vs. temperature for 35 nm CoPc capacitive device (filled symbols). Arrows indicate the thermal cycle direction. Labels A, B, C, and D are reference points for Fig. 2. Inset: Schematic of the Pd/CoPc/Pd device. Note the leveling off of G/A at the lowest T in the cooling branch which indicates the development of microshorts.

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 1×10^{-6} Torr vacuum. In order to avoid high voltage shorts and damage of the sample, the current at each temperature was limited to a 10 μ A maximum. This limits the voltage measurement range, especially at high temperatures where mostly the ohmic region is observed.

Structural characterization as a function of time was carried out using XRD and XRR ($\lambda_{CuK\alpha} = 1.54 \text{ Å}$) in an inert environment chamber in the 80 K–460 K temperature range. Initial structural parameters show that CoPc molecules are oriented parallel to the BE.²⁴

The conductance (G) as a function of temperature (G-T) of a 35 nm OL device is presented in Fig. 1. The data were obtained by measuring the slope G = dI/dV in the ohmic region of the IV curves at each temperature normalized by the active electrode area $(1.8 \times 10^{-4} \text{ cm}^2)$. For each device, the temporal stability at a fixed temperature was established from a minimum of five IV curves recorded every 40 to 50 min. From 40 K to 340 K the devices follow the expected exponential behavior,²³ represented by point A in Fig. 1. At 340 K (point B), G-T noticeably deviates from the exponential behavior and becomes non-monotonic up to 460 K (point C). Upon cooling from 460 K, G depends exponentially on temperature (point D) but with a 3 orders of magnitude lower conductance. The flattening of the conductance below 280 K is due to the presence of microshorts forming metallic bridges through the OL as found earlier.²⁴ These have only weak temperature dependence and become the dominant electrical transport channel at low temperatures.

Up to the irreversibility point B, the IVs show no time dependence. Above point B, the IVs evolve with time to become more asymmetric and less conductive, as shown in Fig. 2(a) (see "B" and "B (after 3h)"). The same time dependence is observed in each measurement with increasing temperature. No time dependence is observed at any temperature as soon as the sample is cooled below 460 K. However, the asymmetry in the IV curves persists with positive voltage branches (positive bias at TE) showing lower conductance (Fig. 2(b)). This indicates that conducting charges (i.e. holes as expected for p-type CoPc) have to overcome a higher potential barrier at the TE/OL interface.

The heating effect was explored in capacitive devices with a broad range of CoPc thicknesses. In order to explore all the devices under the same conditions, a sample with 5 individual devices with 40, 50, 65, 100, and 135 nm thick OLs (Fig. 3, inset) was measured. The G-T of each device is presented in Fig. 3. Below 300 K, all the devices show an exponential behavior with absolute conductance scaling with the device thickness as expected.^{23,24} Above 340 K, the G-T dependence becomes non-monotonic and the exponential behavior recovers only after cooling below 460 K. In this annealed state, the conductance appears mostly independent of device thickness. A second heating cycle after cooling to 280 K reveals a fully reversible "annealed state." In addition, IVs recorded for every device evolve in the same asymmetric fashion as shown in Fig. 2.

The asymmetric IVs for all devices and the appearance of microshorts in the 35 nm CoPc sample suggest that a structural change occurs after heating. To explore this, XRR at each temperature was fitted to a scattering length density (SLD) model using MOTOFIT (Fig. 4).³¹ The software is designed to



FIG. 2. IV curves corresponding to selected points in Fig. 1. (a) Point C (open triangles), initial point B (open squares), and point B after 3h (open circles). (b) Comparison of IVs before (squares, point A) and after annealing (triangles, point D).

easily fit a slab model to a range of datasets, in this case with varying temperature, using the same initial parameter set. Consequently, each fit represents an unbiased model of the structure, which is shown for 300 K in Fig. 4 (inset). The trilayer structure was fitted using fixed SLDs for each material, obtained



FIG. 3. Normalized conductivity (G/A) vs. temperature for Pd/CoPc/Pd capacitive devices with 40, 50, 65, 100, and 135 nm CoPc thickness. The inset shows the schematics of the device.



FIG. 4. (a) XRR (symbols) and fits (lines) of Pd/CoPc/Pd-trilayer as a function of temperature. Inset: SLD profile obtained from the fit at 300 K. (b) Thickness variation of the CoPc layer as a function of temperature obtained from the fitting. Arrows indicate time evolution. Inset: Energy level alignment at the interfaces in the capacitive structure. ϕ_B =barrier for hole injection, $\Delta \phi_B$ =barrier increase due to diffusion and change in average W_{TE} , W_{TE} (W_{BE}) = Top (bottom) electrode work function. All values are referred to the vacuum level.

from single component thin film measurements. Resulting layer thicknesses were 44.4 nm for the TE, 38.0 nm for the OL, and 35.4 nm for the BE, close to the intended device structure of Pd(50 nm)/CoPc(35 nm)/Pd(40 nm)/Al₂O₃-substrate (Fig. 4(a), inset). Note that the TE thickness was reduced with respect to the reported transport devices to allow for better detection with XRR. The BE/OL interface roughness was found to be 1.5 nm and the top of TE roughness was found to be 3 nm. A good fit is obtained by attributing the same roughness to the TE/OL interface; however, this value has a large uncertainty, since the fit was not very sensitive to TE/OL interface roughness (up to an upper limit of 6 nm).

The structural evolution with increasing temperature was investigated by fitting the basic structural model to reflectivity profiles measured at temperatures denoted in Fig. 4(a). The duration of each measurement was 30 min. In addition to the profiles shown, each scan was repeated four times at a constant temperature in order to follow the time evolution. Changes in the reflectivity become visible in the low-Q region below 0.1 Å^{-1} (Fig. 4(a)). In order to limit the number of free parameters in the model, the TE thickness and all SLDs were fixed. The best fit to the data revealed no changes in the BE or roughness parameter. Instead, each

profile could be fitted with a gradually decreasing CoPc layer thickness according to the temperature dependence summarized in Fig. 4(b). Multiple symbols at each temperature show the evolution of the structure with time. The OL thickness reduction can be interpreted as a diffusion of the TE into the OL. Diffusion is expected to affect layer thicknesses, interface roughness, and scattering length densities. However, the density of the OL is very low compared to the Pd layer, so the average of both materials within the diffusion region is close to the Pd density. The interface roughness is not well resolved due to the limited Q-range and the fits match equally well for any roughness up to 6nm. A fitting with both density and thickness being allowed to vary did not lead to consistent results between temperatures. However, each reflectivity can be fitted equally well with the thickness being the only parameter. Unfortunately, the restriction to the fitting avoids absolute quantification of the diffusion process. On the other hand, it prevents false conclusions about the appearance of the interfacial diffusion area. The fitted 10% change of the absolute layer thickness has a clear effect on the XRR profile.

The electrode-OL diffusion was independently confirmed with three different sets of samples consisting of thin film CoPc on Al₂O₃, bilayer structures of CoPc/Pd/Al₂O₃, and Pd/CoPc/Al₂O₃, as well as a trilayer structure of Pd/CoPc/Pd. In all of these samples, the CoPc thickness was 20 nm, while the top and bottom Pd layers were 50 nm and 40 nm, respectively. No changes were observed in the reflectivity with increasing temperature of a single CoPc/Al₂O₃ layer or a bilayer with Pd below the OL (CoPc/Pd/Al₂O₃). Only if Pd was deposited on top of CoPc, heating leads to a change in the structure, which can be reproducibly modeled with a reduced CoPc thickness due to diffusion of the TE.

The diffusion process interpretation of XRR results is supported by the transport measurements. If the CoPc thickness simply decreased, this would lead to an increase in the conductance,²³ which is opposite to the observed behavior (see Figs. 1 and 3). Interdiffused metal ions in the bulk can lead to traps, which introduce a power-law dependence, $I \sim V^{\alpha}$, in the IV characteristic at high bias. A value of $\alpha \sim 3$ obtained indicates the existence of an exponential trap distribution in the device.⁹ The value of α is independent of the heat treatment, which means that the trap distribution in the bulk is not affected by the annealing. Therefore, diffusion effects are mostly limited to the interfacial CoPc/Pd contact area.

XRD revealed a slight preferred orientation of the TE with the (111) direction aligned with the surface normal (Fig. 5). Therefore, the number of planes with orientations different than (111) in contact with the OL is directly proportional to the roughness. With increasing temperature, annealing increases the interdiffusion of Pd into the OL. This process modifies the OL/TE interface leading to increased contact of Pd (110) and (100) surfaces with the OL (Fig. 5, inset). The BE showed strong (111) orientation, with no other orientations being observed along the surface normal. In addition, the BE did not show a temperature dependent diffusion, which indicates an OL/BE interface unaffected by heating.

Studies of the Pd work function show a direct relationship between the metal work function (W_E), crystallographic



FIG. 5. X-ray diffraction (symbols) for a Pd(50 nm)/CoPc(25 nm)/Al₂O₃ bi-layer showing a Pd (111) preferential orientation. The red line shows the simulated Pd powder diffraction without preferential orientation.³³ Inset: Schematic of the diffusion process. Black lines represent the (111) planes. Black arrows show the $\langle 111 \rangle$ orientation. Red arrows indicate the area of non-(111) planes in contact with the organic layer.

contact plane, and roughness.^{25–28} The (111) plane W_E = 5.95 eV, decreases to 5.20 eV for the (110) plane. Since the interdiffusion increases the contact area at the OL/TE interface, this leads to a lower average work function. The barrier for hole injection ϕ_B is given by the difference between the ionization potential of the CoPc (*I*) and the TE work function (W_{TE}).³² This means that a decrease in W_{TE} leads to an increase in the barrier for charge injection into the OL, which decreases the ohmic conductivity. A schematic of the energy levels is shown in Fig. 4(b) (inset). The observed time dependence of the change in transport correlates with the slow temperature activated diffusion observed with x-rays. Furthermore, the results show that interdiffusion decreases with time at a given temperature.

In the IV curves, an increase in conductivity after annealing is observed in the negative branch (see curve D in Fig. 2(b)). This behavior can be explained by different scenarios which are not fully discriminated by the experiments performed. For example, heating can lead to an annealing effect of the BE. A smoother (111) oriented BE/OL interface would increase W_{BE} , which would reduce the BE/OL potential barrier. Such a smoothing of the BE is however not observed in XRR. Moreover, the decrease in W_{TE} can lead to variations in the built-in potential across the device, which shifts the IV curve. Based on the changes in the work function from (111) to (110) oriented surfaces, this shift can amount to a maximum of several 100 mV. Since the TE is not fully (111) oriented (Fig. 5) and the roughness changes by 10 %, the actual change of W_{TE} can be expected to be no more than 10% of the maximum value. Fig. 2(b) is measured over a voltage range exceeding the linear IV dependence. This shows that the measurement range is sufficient to overcome the built-in potential. Preliminary experiments exceeding the ohmic region above 340 K measured in samples with similar layer thicknesses and electrode materials have shown that a maximum 10 μ A current is sufficient to overcome V_{bi} . At higher currents, shorts were observed and the samples were damaged.

In summary, we have investigated the thermal stability of electrical transport in Pd/CoPc/Pd/Al₂O₃-substrate capacitive devices. Heating above the 340 K leads to a non-monotonic conductance dependence on temperature, which leads to an irreversible transition into a 3 orders of magnitude less conductive state. Structural and transport studies indicate that this change originates mostly from interfacial diffusion of the top electrode. This increases the non-(111) OL/TE contact area which decreases the effective TE work function. The temperature determines the amount of diffusion and therefore the change in potential barrier. These results have a direct impact on technological applications since the instabilities of metallic-organic capacitive devices occur at operational temperatures typical for electronic (350 K-400 \text{ K}).

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